What is claimed is:

1. A current cell type digital-to-analog converter comprising:

a current cell matrix including a plurality of upper current cells and at least one lower current cell so as to form a matrix pattern, in which all of the current cells have the same number of constant current transistors connected in parallel, and the constant current transistors are the same size;

an upper control circuit provided within each of the upper current cells for outputting currents of all the constant current transistors within the upper current cell when the upper current cell is selected;

at least one lower control circuit provided within each of the at least one lower current cell for outputting only current of a predetermined number of constant current transistors within the lower current cell when the lower current cell is selected;

a plurality of power supply lines respectively provided in rows of the current cell matrix so that each power supply line supplies currents to the constant current transistors provided in the upper current cell and the lower current cell provided in the corresponding row;

an upper decoder for selecting none or at least one of the upper control circuits in accordance with predetermined one or more upper bits of a digital value;

a lower decoder for selecting none or at least one of

the lower control circuits in accordance with predetermined one or more lower bits of the digital value; and

an analog output terminal for outputting a summation of output currents of the upper current cells and the at least one lower current cell.

2. The current cell type digital-to-analog converter according to claim 1, wherein the at least one lower control circuit of each of the at least one lower current cell includes a plurality of lower control circuits, and the plurality of lower control circuits cause the constant current transistors of the lower current cell concerned to output different number of currents.

3. The current cell type digital-to-analog converter according to claim 1, wherein each of the at least one lower current cell includes at least one dummy constant current transistor for equalizing the number of said constant current transistors with the number of said upper current cells, and the dummy constant current transistor discharges current supplied from the power supply line to a ground line.

4. The current cell type digital-to-analog converter according to claim 1, wherein the upper decoder alternately selects the current cells from both ends of a row when a plurality of the upper current cells are simultaneously selected within the same row.

5. The current cell type digital-to-analog converter according to claim 4, wherein the at least one lower current cell is provided at a position in the last row which

corresponds to the positions of the upper current cells selected last in other rows.

6. The current cell type digital-to-analog converter according to claim 1, wherein the constant current transistors are pMOS transistors.

7. The current cell type digital-to-analog converter according to claim 1, wherein the upper control circuit includes a gating pMOS transistor, a diode-connected nMOS transistor, an OR gate, an AND gate and an inverter.

8. The current cell type digital-to-analog converter according to claim 1, wherein the lower control circuit includes a plurality of gating pMOS transistors, a plurality of diode-connected nMOS transistors, and a plurality of inverters.

9. The current cell type digital-to-analog converter according to claim 7, wherein the inverter has a CMOS structure.

10. The current cell type digital-to-analog converter according to claim 8, wherein the inverter has a CMOS structure.

11. The current cell type digital-to-analog converter according to claim 1 further including a latch which latches select signals output from the upper decoder and the lower decoder.

12. The current cell type digital-to-analog converter according to claim 11, wherein the latch supplies one column select signal and two row select signals to each of the upper

current cells via respective select signal lines, and supplies a plurality of select signals to each of the at least one lower current cell via respective select signal lines.

13. A current cell type digital-to-analog converter comprising:

matrix means including a plurality of upper current cells and at least one lower current cell so as to form a matrix pattern, in which all of the current cells have the same number of constant current transistors connected in parallel, and the constant current transistors are the same size;

first means provided within each of the upper current cells for outputting currents of all the constant current transistors within the upper current cell when the upper current cell is selected;

at least one second means provided within each of the at least one lower current cell for outputting only current of a predetermined number of constant current transistors within the lower current cell when the lower current cell is selected;

a plurality of third means respectively provided in rows of the matrix means so that each third means supplies currents to the constant current transistors provided in the upper current cell and the lower current cell provided in the corresponding row;

fourth means for selecting none or at least one of the first means in accordance with predetermined one or more upper bits of a digital value;

fifth means for selecting none or at least one of the second means in accordance with predetermined one or more lower bits of the digital value; and

sixth means for outputting a summation of output currents of the upper current cells and the at least one lower current cell.

14. The current cell type digital-to-analog converter according to claim 13, wherein the at least one second means of each of the at least one lower current cell includes a plurality of second means, and the plurality of second means cause the constant current transistors of the lower current cell concerned to output different number of currents.

15. The current cell type digital-to-analog converter according to claim 13, wherein each of the at least one lower current cell includes at least one dummy constant current transistor for equalizing the number of said constant current transistors with the number of said upper current cells, and the dummy constant current transistor discharges current supplied from the third means to a ground line.

16. The current cell type digital-to-analog converter according to claim 13, wherein the fourth means alternately selects the current cells from both ends of a row when a plurality of the upper current cells are simultaneously selected within the same row.

17. The current cell type digital-to-analog converter according to claim 16, wherein the at least one lower current cell is provided at a position in the last row which

corresponds to the positions of the upper current cells selected last in other rows.

18. The current cell type digital-to-analog converter according to claim 13, wherein the constant current transistors are pMOS transistors.

19. The current cell type digital-to-analog converter according to claim 13, wherein the first means includes a gating pMOS transistor, a diode-connected nMOS transistor, an OR gate, an AND gate and an inverter.

20. The current cell type digital-to-analog converter according to claim 13, wherein the second means includes a plurality of gating pMOS transistors, a plurality of diode-connected nMOS transistors, and a plurality of inverters.